THAT WHICH IS CLAIMED IS:

1. A solid state image sensor comprising a doped single crystal chip, one face of the chip forming an active pixel array; said face being formed on a P substrate by a P-epitaxial layer on which are formed pixels each comprising:

an N-well acting as a collection node, one or more P-wells adjacent the N-well, and

in-pixel circuit elements comprising as active elements only NMOS transistors in at least one said P-well.

2. A solid state image sensor as defined in claim 1 but with N and P reversed.

3. An image sensor according to claim 1 or claim 2, in which said in-pixel circuit elements form part of an analog-to-digital converter which also comprises circuit elements external to the pixel.

4. An image sensor according to claim 3, in which said in-pixel circuit elements form an amplifier which is connected, directly or by switching, to a comparator external to the pixel and forming part of the analog to digital converter.

5. An image sensor according to claim 4, in which the in-pixel circuit elements form a long tail pair connected to receive the pixel photodiode voltage and a reference voltage, and providing a balanced output to an off-pixel current mirror which in turn is connected to said comparator.

6. An image sensor according to claim 5, including a counter in which a count is latched by a change of state of the comparator.

7. An image sensor according to claim 6, including a frame store, and in which the count latched in the counter is transferred to the frame store.

8. An image sensor according to claim 5, in which the reference voltage is ramped during the time when the photodiode is integrating photoinduced current.

9. An image sensor according to claim 5 or claim 8, in which the reference voltage is ramped during reset of the pixel to provide offset compensation.

10. An image sensor according to claim 6 or claim 7, in which each pixel is provided with a respective off-pixel comparator and counter.

11. An image sensor according to claim 6 or claim 7, in which a number of pixels in a given row or column share a single off-pixel comparator and counter, said pixels being enabled sequentially.

12. An image sensor according to claim 11, in which the outputs of the long tail pair in each pixel are multiplexed to a pair of output lines common to said number of pixels.

13. An image sensor according to claim 11 or

claim 12, in which cascode transistors are provided in the outputs of each long tail pair.